

CLAIMS

1. A non-volatile latch circuit comprising:
 - a ferroelectric capacitor having a first
5 electrode , a second electrode , and a ferroelectric film
disposed between the first electrode and the second
electrode;
a first input terminal for applying a voltage to
the first electrode;
10 an inverter element having an input portion and
an output portion, the input portion being connected to
the second electrode of the ferroelectric capacitor;
a second input terminal for applying a voltage
to the second electrode;
15 a switching element connected between the
second electrode and the second input terminal for
switching the voltage applied to the second electrode;
and
a third input terminal for applying a voltage to
20 the switching element to change the on/off-state thereof;
the inverter element outputting a high-level
voltage to the output portion when a low-level voltage,
which is lower than the threshold of the inverter element,
is applied to the input portion thereof, and outputting a
25 low-level voltage to the output portion when a high-level

voltage, which is higher than the threshold of the inverter element, is applied to the input portion thereof;

the voltage that is generated at the second
5 electrode by residual polarization in the ferroelectric film being higher than the threshold voltage of the inverter element when the voltage is applied to the first input terminal and the switching element is turned off.

10 2. A non-volatile latch circuit according to Claim 1,

wherein the inverter element is composed of a complementary MOS inverter element comprising a first MISFET and a second MISFET;

15 the first MISFET comprises a first gate electrode, a first gate insulating film, a first source region, and a first drain region;

the second MISFET comprises a second gate electrode, a second gate insulating film, a second source
20 region, and a second drain region;

the first gate electrode and the second gate electrode are connected to the input portion;

the first drain region and the second drain region are connected to the output portion;

25 a voltage is applied to the first source

region in such a manner that the first source region has a high potential;

a voltage is applied to the second source region in such a manner that the second source region has
5 a low potential;

the first MISFET is turned on when a low-level voltage, which is lower than the threshold of the inverter element, is applied to the input portion, and turned off when a high-level voltage, which is higher
10 than the threshold of the inverter element, is applied to the input portion, and

the second MISFET is turned on when a high-level voltage, which is higher than threshold of the inverter element, is applied to the input portion, and
15 turned off when a low-level voltage, which is lower than the threshold of the inverter element, is applied to the input portion.

3. A non-volatile latch circuit according to
20 Claim 2, wherein the threshold voltage of the second MISFET is the threshold voltage of the inverter element.

4. A non-volatile latch circuit according to Claim 2, wherein the first MISFET is p-type and the
25 second MISFET is n-type.

5. A non-volatile latch circuit according to Claim 2, wherein the voltage that makes the first source region high potential is positive supply voltage.

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6. A non-volatile latch circuit according to Claim 2, wherein the voltage that makes the second source region low potential is earth voltage.

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7. A non-volatile latch circuit according to Claim 1, wherein the low-level voltage, which is lower than the threshold of the inverter element, is an earth voltage.

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8. A non-volatile latch circuit according to Claim 1, wherein the ferroelectric film is formed of strontium bismuth tantalate.

20 9. A method for driving a non-volatile latch circuit that comprises:

a ferroelectric capacitor having a first electrode, a second electrode, and a ferroelectric film disposed between the first electrode and the second electrode;

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a first input terminal for applying a voltage to

the first electrode;

an inverter element having an input portion and an output portion, the input portion being connected to the second electrode of the ferroelectric capacitor;

5 a second input terminal for applying a voltage to the second electrode;

a switching element connected between the second electrode and the second input terminal for switching the voltage applied to second electrode; and

10 a third input terminal for applying a voltage to the switching element to change the on/off state thereof;

the inverter element outputting a high-level voltage to the output portion when a low-level voltage, which is lower than the threshold of the inverter element, is applied to the input portion thereof, and outputting a low-level voltage to the output portion when a high-level voltage, which is higher than the threshold of the inverter element, is applied to the input portion thereof,

15 the high-level voltage being applied to the first input terminal while the switching element is kept in the off state; and

the voltage that is generated at second electrode by residual polarization in the ferroelectric film when a low-level voltage is sequentially applied being higher than the threshold voltage of the inverter

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element;

the method for driving the non-volatile latch circuit also comprising a high-level latch step, a low-level latch step, and a reset step;

5 the high-level latch step having a first write substep followed by a first read substep, wherein

in the first write substep, a low-level voltage, which is lower than the threshold of the inverter element, is applied to the second input terminal, and a high-level
10 voltage is applied to the third input terminal to turn on the switching element, so that the voltage applied to the input portion is made a low-level voltage that is lower than the threshold of the inverter element, and

in the first read substep, the voltage that is
15 applied to the input portion is kept at a level that is lower than the threshold of the inverter element;

the low-level latch step having a second write substep followed by a second read substep, wherein

in the second write substep, a high-level
20 voltage is applied to the first input terminal to generate a high-level voltage that is higher than the threshold of the inverter element in the input portion, while the switching element is tuned off by applying a low-level voltage to the third input terminal, and

25 in the second read substep, a high-level

voltage, which is higher than the threshold of the inverter element, is kept in the input portion while the switching element is maintained in an off state; and

in the reset step, a low-level voltage that is
5 lower than the threshold of the inverter element is applied to the second input terminal, and the switching element is turned on.

10. A method for driving a non-volatile latch
10 circuit according to Claim 9, wherein the second write substep comprises the steps of:

applying a low-level voltage, which is lower than the threshold of the inverter element, to the second input terminal and making the switching element into an
15 on state,

applying a high-level voltage to the first input terminal while keeping the switching element in an on state, and

turning off the switching element under the
20 condition where a high-level voltage is applied to the first input terminal.

11. A method for driving a non-volatile latch circuit according to Claim 10, wherein the first write
25 substep comprises the steps of:

making the switching element into an on state while applying a low-level voltage, which is lower than the threshold of the inverter element, to the second input terminal, and applying a high-level voltage to the
5 third input terminal,

applying a high-level voltage, which is higher than the threshold of the inverter element, to the second input terminal while keeping the switching element in an on state, and

10 applying a low-level voltage, which is lower than the threshold of the inverter element, while keeping the switching element in an on state.

12. A method for driving a non-volatile latch
15 circuit according to Claim 9, wherein the inverter element is formed of a complementary MOS inverter element composed of a first MISFET and a second MISFET,

the first MISFET comprises a first gate electrode, a first gate insulating film, a first source
20 region, and a first drain region,

the second MISFET comprises a second gate electrode, a second gate insulating film, a second source region, and a second drain region,

the first gate electrode and the second gate
25 electrode are connected to the input portion,

the first drain region and the second drain region are connected to the output portion,

a voltage is applied to the first source region in such a manner that the first source region has a high potential,

a voltage is applied to the second source region in such a manner that the second source region has a low potential,

the first MISFET becomes on when a low-level voltage, which is lower than the threshold of the inverter element, is applied to the input portion, and becomes off when a high-level voltage, which is higher than the threshold of the inverter element, is applied to the input portion,

the second MISFET becomes on when a high-level voltage, which is higher than the threshold of the inverter element, is applied to the input portion, and becomes off when a low-level voltage, which is lower than the threshold of the inverter element, is applied to the input portion.

13. A method for driving a non-volatile latch circuit according to Claim 12, wherein the threshold voltage of the second MISFET is the threshold voltage of the inverter element.

14. A method for driving a non-volatile latch circuit according to Claim 12, wherein the first MISFET is p-type and the second MISFET is n-type.

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15. A method for driving a non-volatile latch circuit according to Claim 12, wherein the voltage that makes the first source region high potential is a positive supply voltage.

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16. A method for driving a non-volatile latch circuit according to Claim 12, wherein the voltage that makes the second source region low potential is an earth voltage.

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17. A method for driving a non-volatile latch circuit according to Claim 9, wherein the low-level voltage, which is lower than the threshold of the inverter element, is an earth voltage.

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18. A method for driving a non-volatile latch circuit according to Claim 9, wherein the ferroelectric film is formed of strontium bismuth tantalate.

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19. A method for driving a non-volatile latch

circuit according to Claim 9, wherein the high-level voltage applied to the first input terminal is higher than the high-level voltage that is applied to the third input terminal.

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20. A method for driving a non-volatile latch circuit according to Claim 9, wherein during the first read substep, a voltage lower than the threshold of the inverter element is applied to the first input terminal.

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21. A method for driving a non-volatile latch circuit according to Claim 20, wherein the low-level voltage, which is lower than the threshold of the inverter element is an earth voltage.